

HM51W4260A/AL Series

Preliminary

262,144-word × 16-bit Dynamic Random Access Memory

The Hitachi HM51W4260A/AL are CMOS dynamic RAM organized as 262,144-word × 16-bit. HM51W4260A/AL have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM51W4260A/AL offer fast page mode as a high speed access mode.

Multiplexed address input permits the HM51W4260A/AL to be packaged in standard 400-mil 40-pin plastic TSOPII.

Internal refresh timer enables self refresh operation.

Features

- Single 3.3 V (± 0.3 V)
- High speed
 - Access time: 70 ns/80 ns/100 ns (max)
- Low power dissipation
 - Active mode: 396 mW/342 mW/306 mW (max)
 - Standby mode: 7.2 mW (max)
0.36 mW (max) (L-version)
- Fast page mode capability
- 512 refresh cycles: 8 ms
128 ms (L-version)
- 2 $\overline{\text{CAS}}$ byte control
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - CAS-before- $\overline{\text{RAS}}$ refresh
- Battery back up operation (L-version)
- Self-refresh operation

Ordering Information

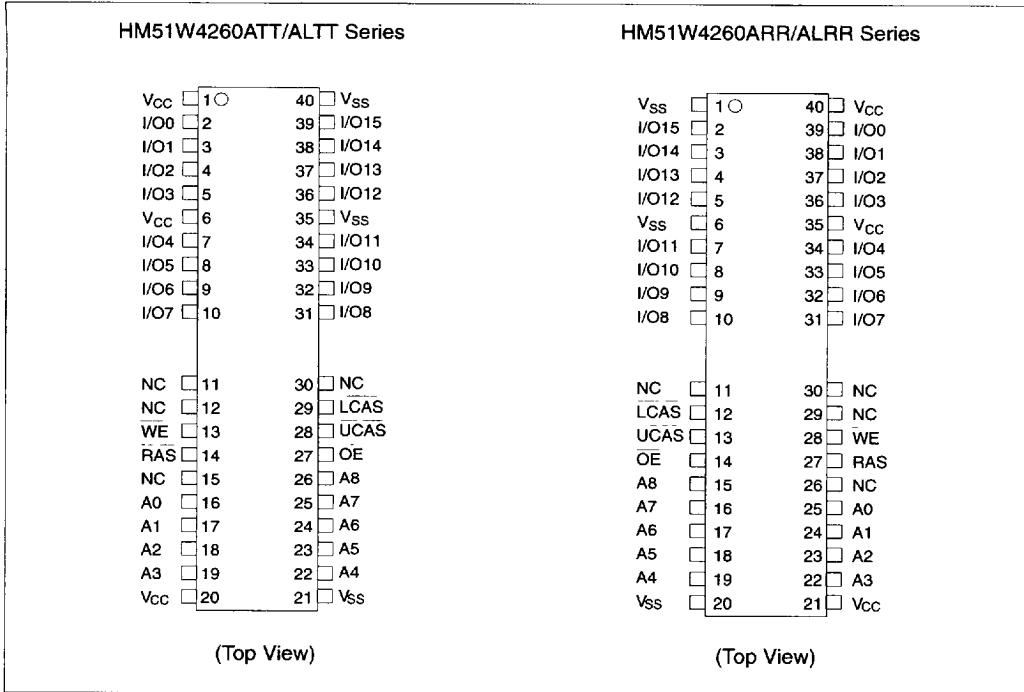
Type No.	Access time	Package
HM51W4260ATT-7	70 ns	400-mil 40-pin plastic TSOPII
HM51W4260ATT-8	80 ns	(TTP-40DB)
HM51W4260ATT-10	100 ns	
HM51W4260ALTT-7	70 ns	400 mil 40-pin plastic TSOPII
HM51W4260ALTT-8	80 ns	(TTP-40DB)
HM51W4260ALTT-10	100 ns	
HM51W4260ARR-7	70 ns	400 mil 40-pin plastic TSOPII
HM51W4260ARR-8	80 ns	(TTP-40DB)
HM51W4260ARR-10	100 ns	
HM51W4260ALRR-7	70 ns	400 mil 40-pin plastic TSOPII
HM51W4260ALRR-8	80 ns	(TTP-40DB)
HM51W4260ALRR-10	100 ns	

Note : The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

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Pin Arrangement



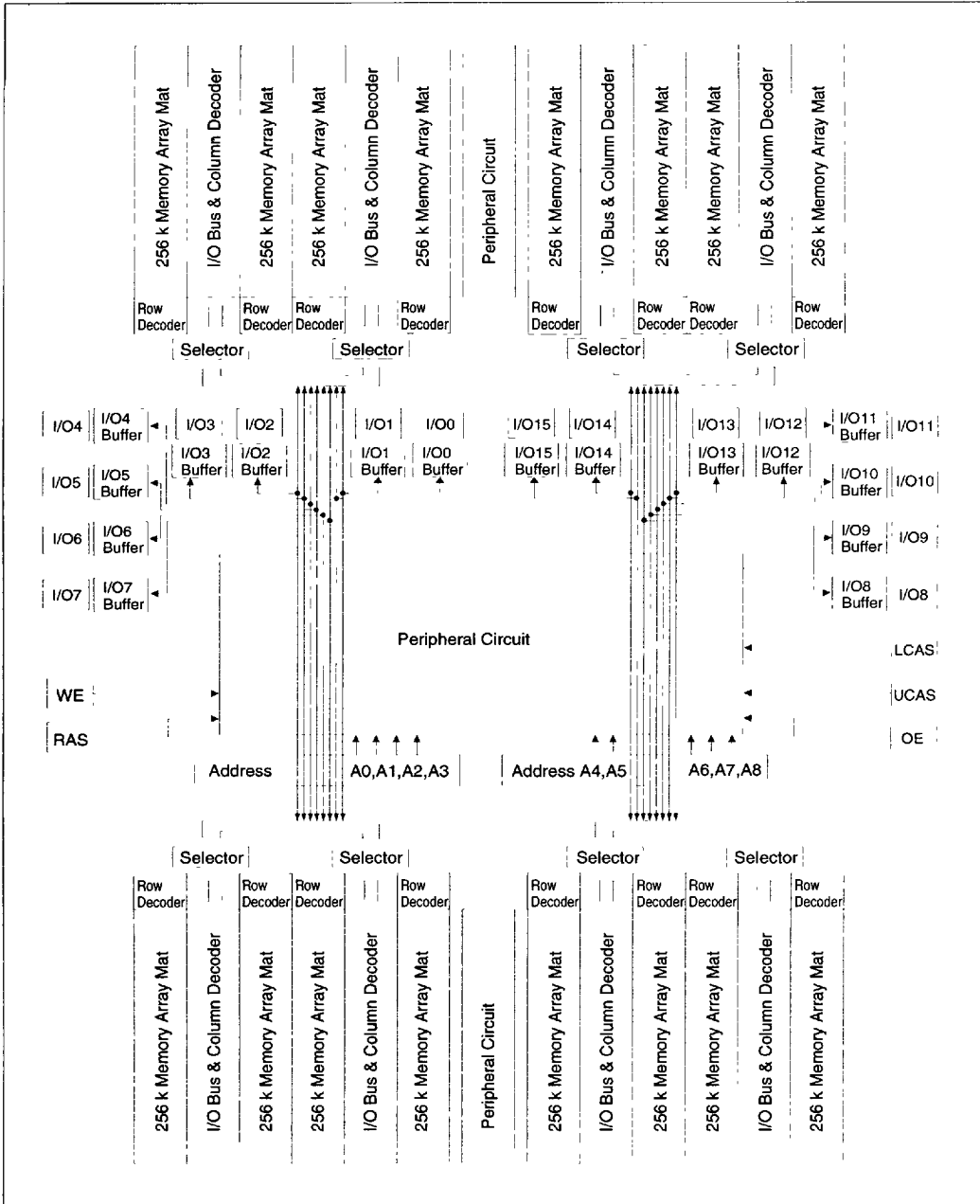
Pin Description

Pin name	Function
A0 – A8	Address input – Row address A0 – A8 – Column address A0 – A8 – Refresh address A0 – A8
I/O0 – I/O15	Data-in/data-out
RAS	Row address strobe
UCAS, LCAS	Column address strobe
WE	Read/write enable
OE	Output enable
V _{CC}	Power (+3.3 V)
V _{SS}	Ground

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Block Diagram



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Truth Table

Inputs					I/O		Operation
RAS	LCAS	UCAS	WE	OE	I/O0 – I/O7	I/O8 – I/O15	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	
H to L	L	H	–	–	High-Z	High-Z	CBR refresh or Self refresh
H to L	H	L	–	–	High-Z	High-Z	
H to L	L	L	–	–	High-Z	High-Z	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _T	–0.5 to +4.6	V
Supply voltage relative to V _{SS}	V _{CC}	–0.5 to +4.6	V
Short circuit output current	I _{out}	50	mA
Power dissipation	P _T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

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Recommended DC Operating Conditions (Ta = 0 to +70°C) *2

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{SS}	0	0	0	V	2
	V _{CC}	3.0	3.3	3.6	V	1, 2
Input high voltage	V _{IH}	2.0	—	V _{CC} +0.3	V	1
Input low voltage	V _{IL}	-0.3	—	0.8	V	1

- Notes: 1. All voltage referred to V_{SS}
 2. The supply voltage with all V_{CC} pins must be on the same level.
 The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	HM51W4260A /AL-7		HM51W4260A /AL-8		HM51W4260A /AL-10		Unit	Testconditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	110	—	95	—	85	mA	RAS cycling LCAS or UCAS cycling t _{RC} = min	1, 2
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, LCAS, UCAS = V _{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface RAS, LCAS, UCAS, WE OE ≥ V _{CC} - 0.2 V Dout = High-Z	
Standby current (L-version)		—	100	—	100	—	100	μA	CMOS interface RAS, LCAS, OE, WE UCAS ≥ V _{CC} - 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	105	—	92	—	75	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	5	—	5	—	5	mA	RAS = V _{IH} LCAS or UCAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	105	—	92	—	75	mA	t _{RC} = min	2
Fast page mode current	I _{CC7}	—	95	—	80	—	75	mA	t _{PC} = min	1, 3

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (cont)

Parameter	Symbol	HM51W4260A /AL-7		HM51W4260A /AL-8		HM51W4260A /AL-10		Unit	Testconditions	Notes
		Min	Max	Min	Max	Min	Max			
Battery back up current (Standby with CBR refresh) (L-version)	I _{CC10}	—	100	—	100	—	100	μA	Standby: CMOS interface 4 Dout = High-Z CBR refresh: $t_{RC} = 250 \mu s$ $t_{RAS} \leq 1 \mu s$, \overline{LCAS} , $\overline{UCAS} = V_{IL}$ WE, OE = V _{IH}	
Self-refresh mode current	I _{CC11}	—	1	—	1	—	1	mA	CMOS interface \overline{RAS} , \overline{LCAS} , $\overline{UCAS} \leq 0.2 V$, Dout = High-Z	
Self-refresh mode current (L-version)		—	100	—	100	—	100	μA	CMOS interface \overline{RAS} , \overline{LCAS} , $\overline{UCAS} \leq 0.2 V$, Dout = High-Z	
Input leakage current	I _{LI}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I _{LO}	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -2.0 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2.0 mA	

- Notes:
1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while \overline{LCAS} and $\overline{UCAS} = V_{IH}$.
 4. $V_{IH} \geq V_{CC} - 0.2 V$, $0 \leq V_{IL} \leq 0.2 V$, Address can be changed once or less while \overline{LCAS} and $\overline{UCAS} = V_{IL}$.
 5. All the V_{CC} pins shall be supplied with the same voltage. And all the V_{SS} pins shall be supplied with the same voltage.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	5	pF	1
Input capacitance (Clocks)	C _{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	C _{I/O}	—	10	pF	1, 2

- Notes:
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. \overline{LCAS} and $\overline{UCAS} = V_{IH}$ to disable Dout.

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AC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$) *1, *14, *15, *17, *18

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM51W4260A /AL-7		HM51W4260A /AL-8		HM51W4260A /AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130	—	150	—	180	—	ns	
\overline{RAS} precharge time	t_{RP}	50	—	60	—	70	—	ns	
\overline{RAS} pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
\overline{CAS} pulse width	t_{CAS}	20	10000	20	10000	25	10000	ns	23
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	19
Column address hold time	t_{CAH}	15	—	15	—	20	—	ns	19
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	50	20	60	25	75	ns	8
\overline{RAS} to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	9
\overline{RAS} hold time	t_{RSH}	20	—	20	—	25	—	ns	
\overline{CAS} hold time	t_{CSH}	70	—	80	—	100	—	ns	
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	10	—	10	—	10	—	ns	20
\overline{OE} to Din delay time	t_{ODD}	20	—	20	—	25	—	ns	
\overline{OE} delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
\overline{CAS} setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	HM51W4260A /AL-7		HM51W4260A /AL-8		HM51W4260A /AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	70	—	80	—	100	ns	2, 27
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	20	—	20	—	25	ns	4, 13, 27
Access time from address	t_{AA}	—	35	—	40	—	45	ns	5, 13, 27
Access time from $\overline{\text{OE}}$	t_{OAC}	—	20	—	20	—	25	ns	23, 27
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	19
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	16, 19
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	16
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output buffer turn-off to $\overline{\text{OE}}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM51W4260A /AL-7		HM51W4260A /AL-8		HM51W4260A /AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10, 19
Write command hold time	t_{WCH}	15	—	15	—	20	—	ns	19
Write command pulse width	t_{WP}	10	—	10	—	20	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	20	—	20	—	25	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	20	—	20	—	25	—	ns	21
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	20	—	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ delay time	t_{COD}	—	0	—	0	—	0	ns	23

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Read-Modify-Write Cycle

Parameter	Symbol	HM51W4260A /AL-7		HM51W4260A /AL-8		HM51W4260A /AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	180	—	200	—	245	—	ns	
\overline{RAS} to \overline{WE} delay time	t_{RWD}	95	—	105	—	135	—	ns	10
\overline{CAS} to \overline{WE} delay time	t_{CWD}	45	—	45	—	60	—	ns	10
Column address to \overline{WE} delay time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
\overline{OE} hold time from \overline{WE}	t_{OEh}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM51W4260A /AL-7		HM51W4260A /AL-8		HM51W4260A /AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
\overline{CAS} setup time (\overline{CAS} -before- \overline{RAS} refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	19
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	20
\overline{RAS} precharge to \overline{CAS} hold time	t_{RPC}	10	—	10	—	10	—	ns	19
\overline{CAS} precharge time in normal mode	t_{CPN}	10	—	10	—	10	—	ns	22

Fast Page Mode Cycle

Parameter	Symbol	HM51W4260A /AL-7		HM51W4260A /AL-8		HM51W4260A /AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
Fast page mode \overline{CAS} precharge time	t_{CP}	10	—	10	—	10	—	ns	22
Fast page mode \overline{RAS} pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from \overline{CAS} precharge	t_{ACP}	—	40	—	45	—	50	ns	13, 20, 27
\overline{RAS} hold time from \overline{CAS} precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast page mode read-modify-write cycle \overline{CAS} precharge to WE delay time	t_{CPW}	65	—	70	—	85	—	ns	
Fast page mode read-modify-write cycle time	t_{PCM}	95	—	100	—	110	—	ns	

Self-refresh Mode

Parameter	Symbol	HM51W4260A /AL-7		HM51W4260A /AL-8		HM51W4260A /AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
\overline{RAS} pulse width (self-refresh)	t_{RASS}	100	—	100	—	100	—	μs	
\overline{RAS} precharge time (self-refresh)	t_{RPS}	130	—	150	—	180	—	ns	
\overline{CAS} hold time (self-refresh)	t_{CHS}	-50	—	-50	—	-50	—	ns	21

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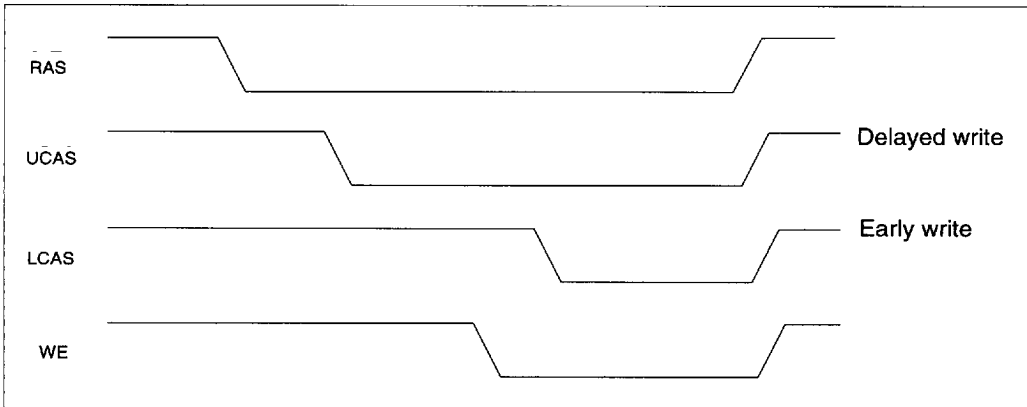
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- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referred to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
 12. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
 14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
 15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 17. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ cannot be staggered within the same write/read cycles.
 18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 19. t_{ASC} , t_{CAH} , t_{RCS} , t_{RCH} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 20. t_{CRP} , t_{CHR} , t_{ACP} and t_{CPW} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 21. t_{CWL} , t_{DH} , t_{DS} and t_{CHS} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 22. t_{CPN} and t_{CP} are determined by the time that both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.
 23. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH}(\text{min})/V_{IL}(\text{max})$ level.
 24. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
 25. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
 26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
 27. Measured with a load equivalent to 1 TTL load and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).

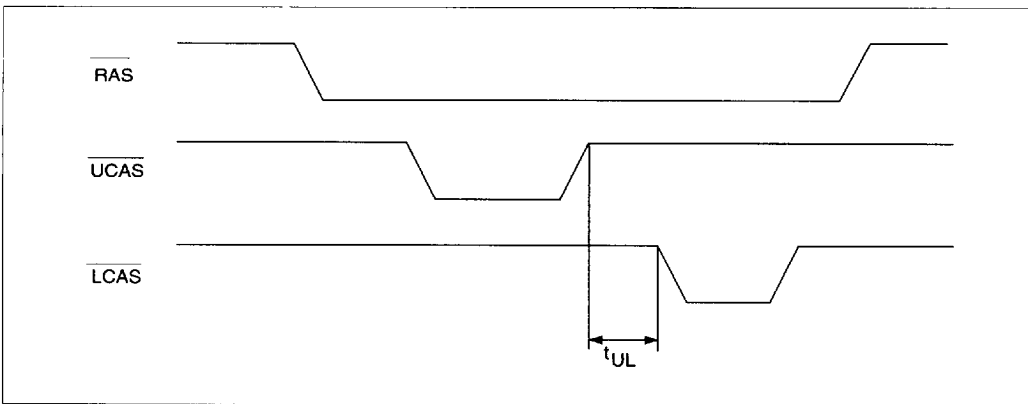
Notes concerning 2 CAS control

Please do not separate the $\overline{UCAS}/\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}/\overline{LCAS}$ are allowed under the following conditions.

- (1) Each of the $\overline{UCAS}/\overline{LCAS}$ should satisfy the timing specifications individually.
- (2) Different operation mode for upper/lower byte is not allowed; such as following.



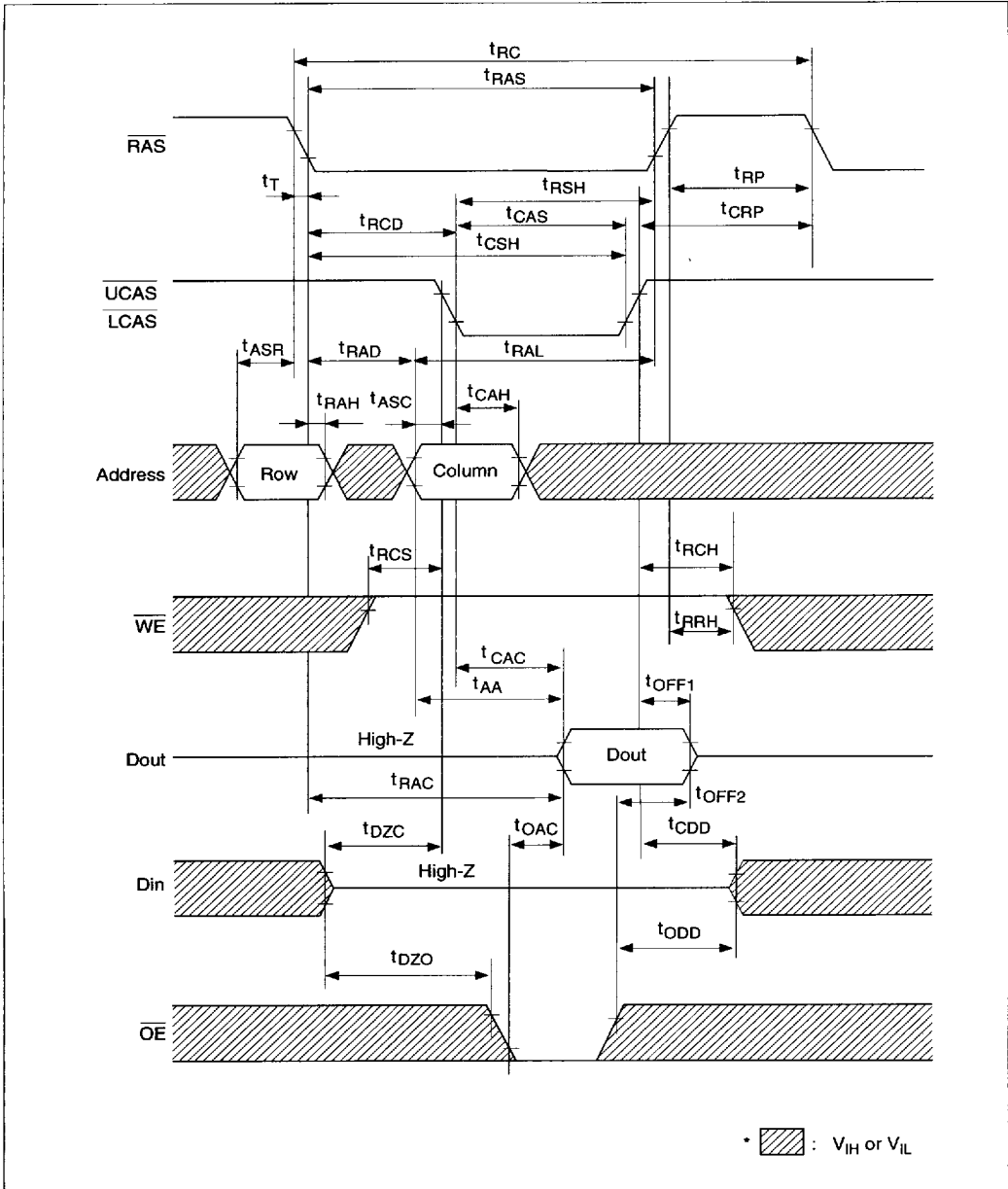
- (3) Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} < t_{UL}$) is satisfied, fast page mode can be performed.



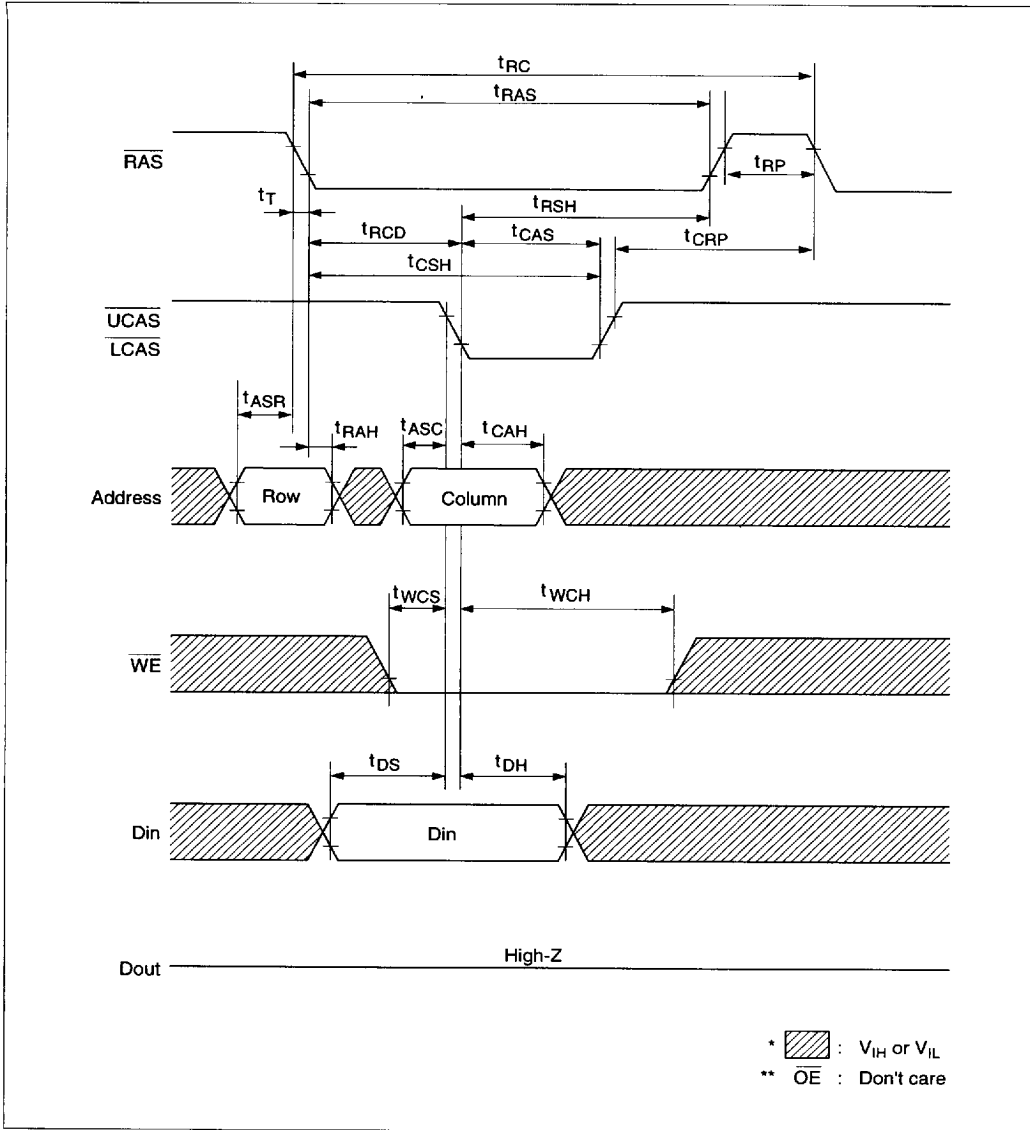
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Timing Waveforms

Read Cycle



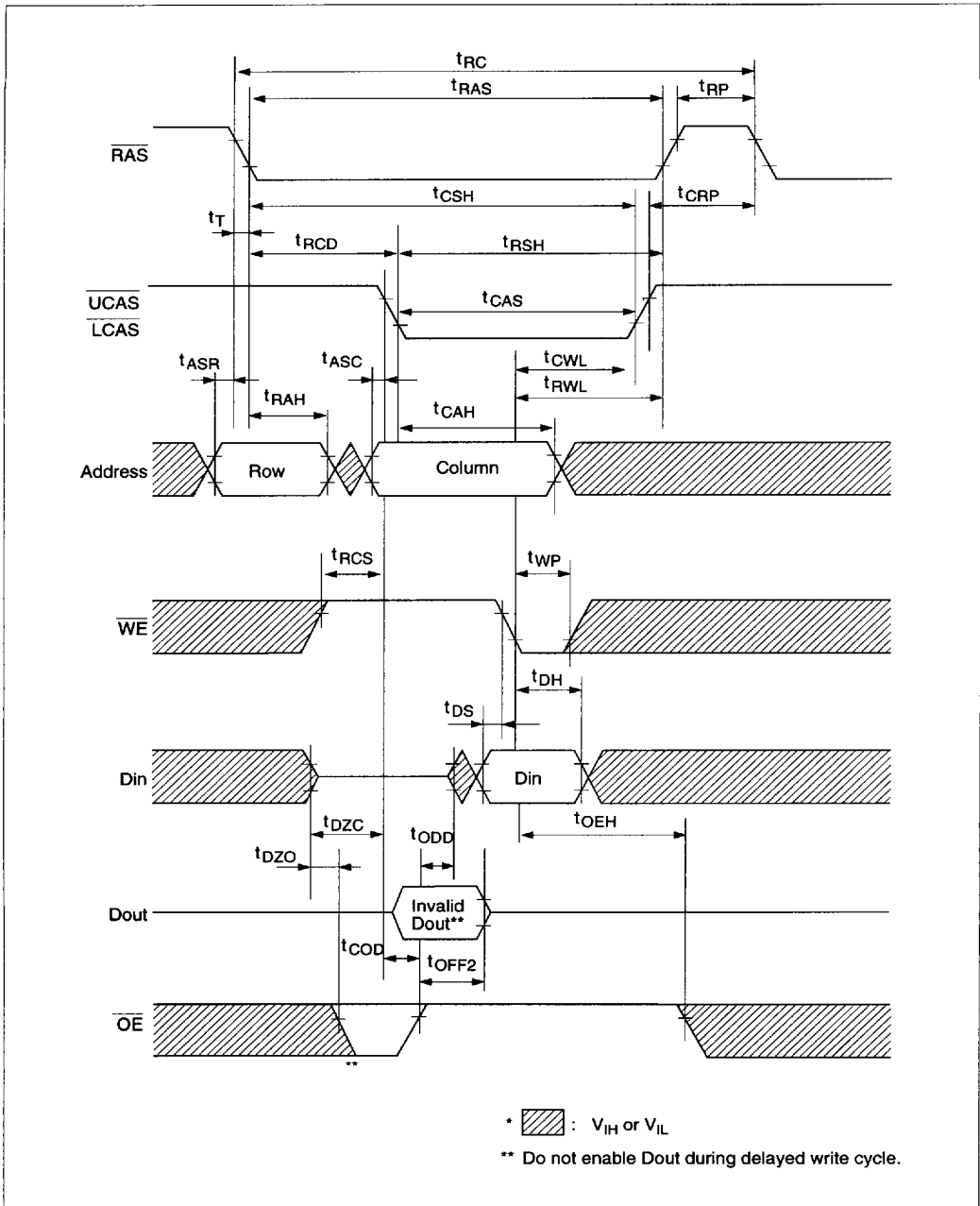
Early Write Cycle



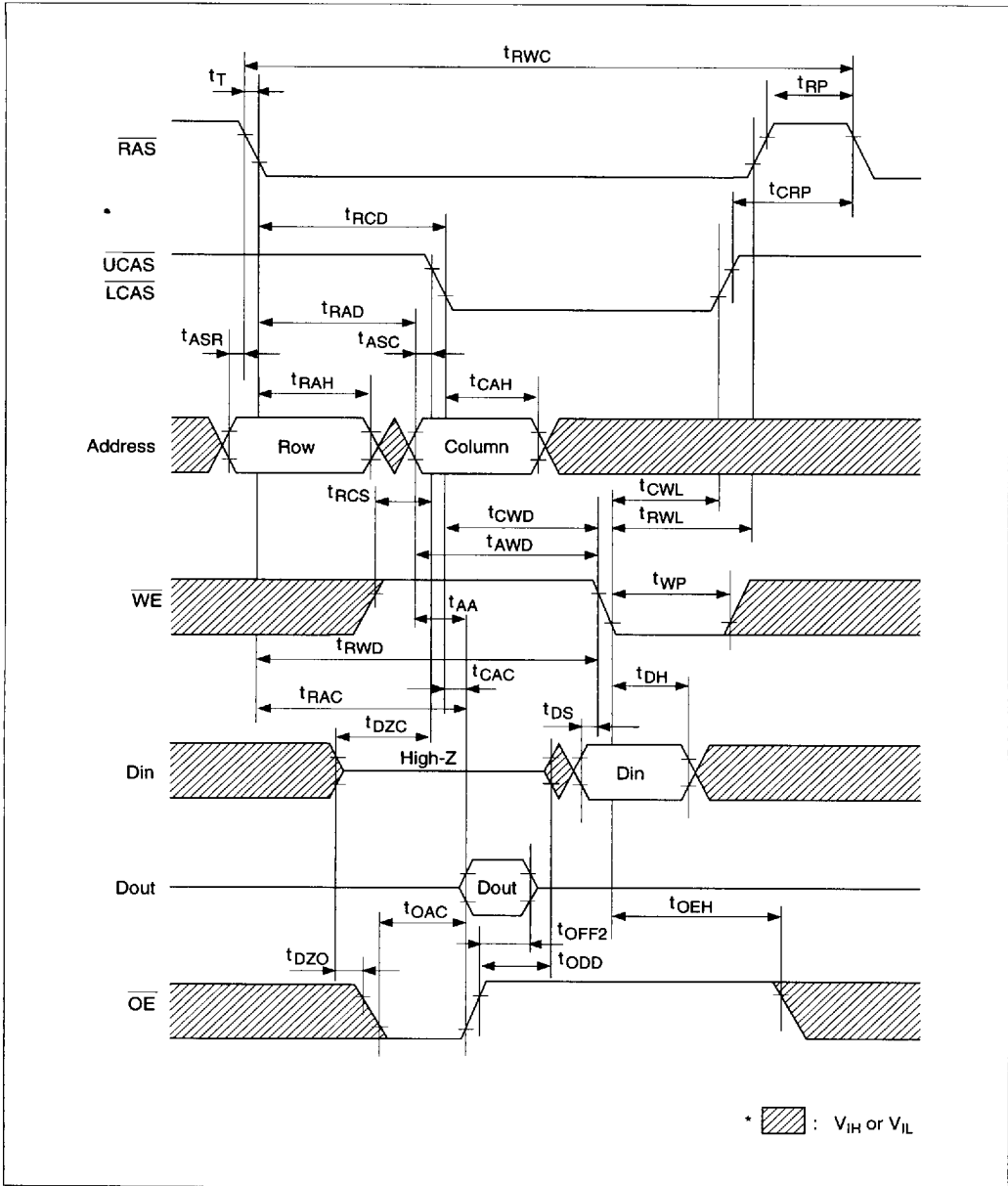
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Delayed Write Cycle

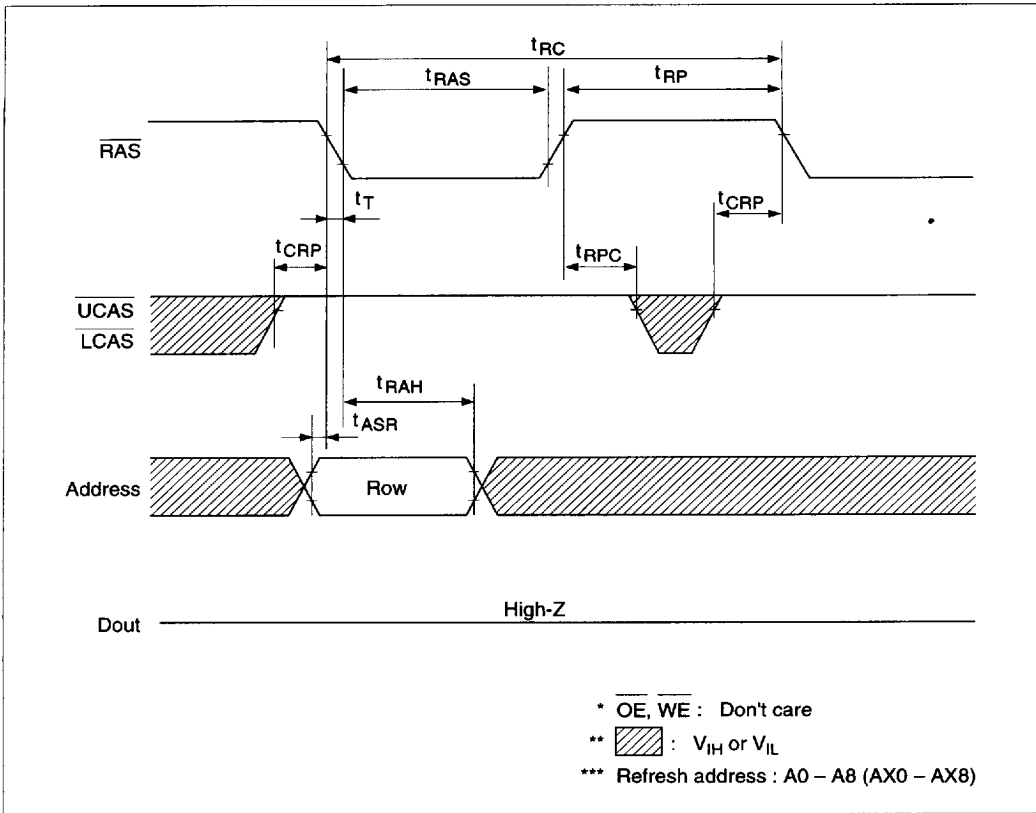


Read-Modify-Write Cycle

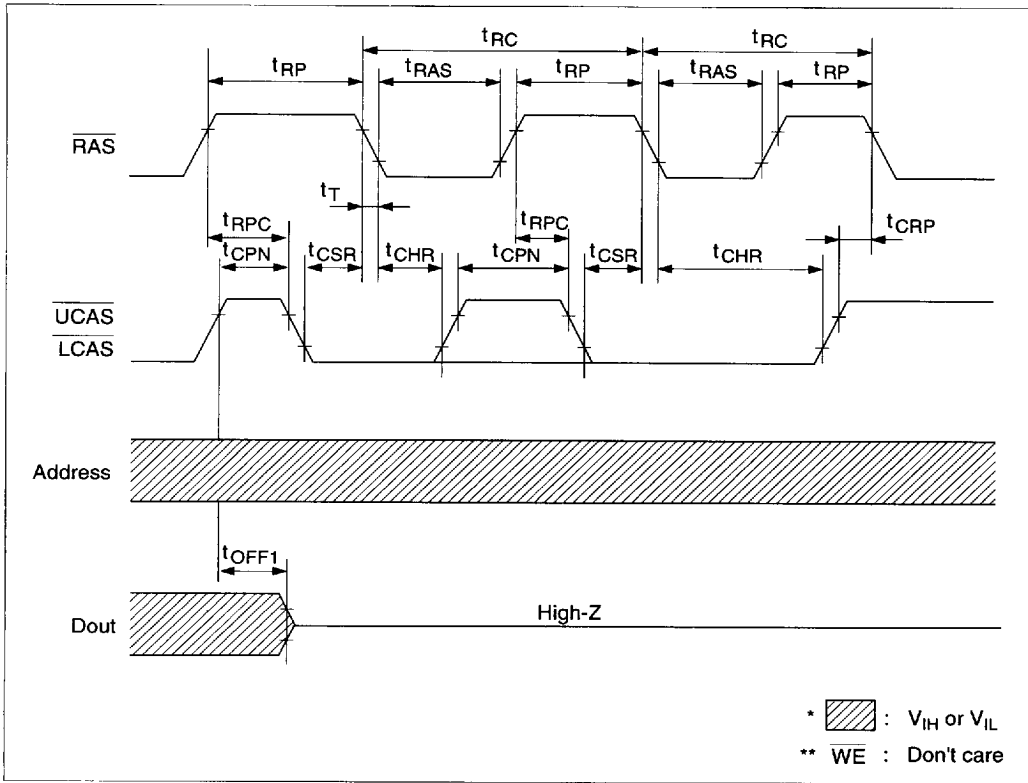


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RAS-Only Refresh Cycle



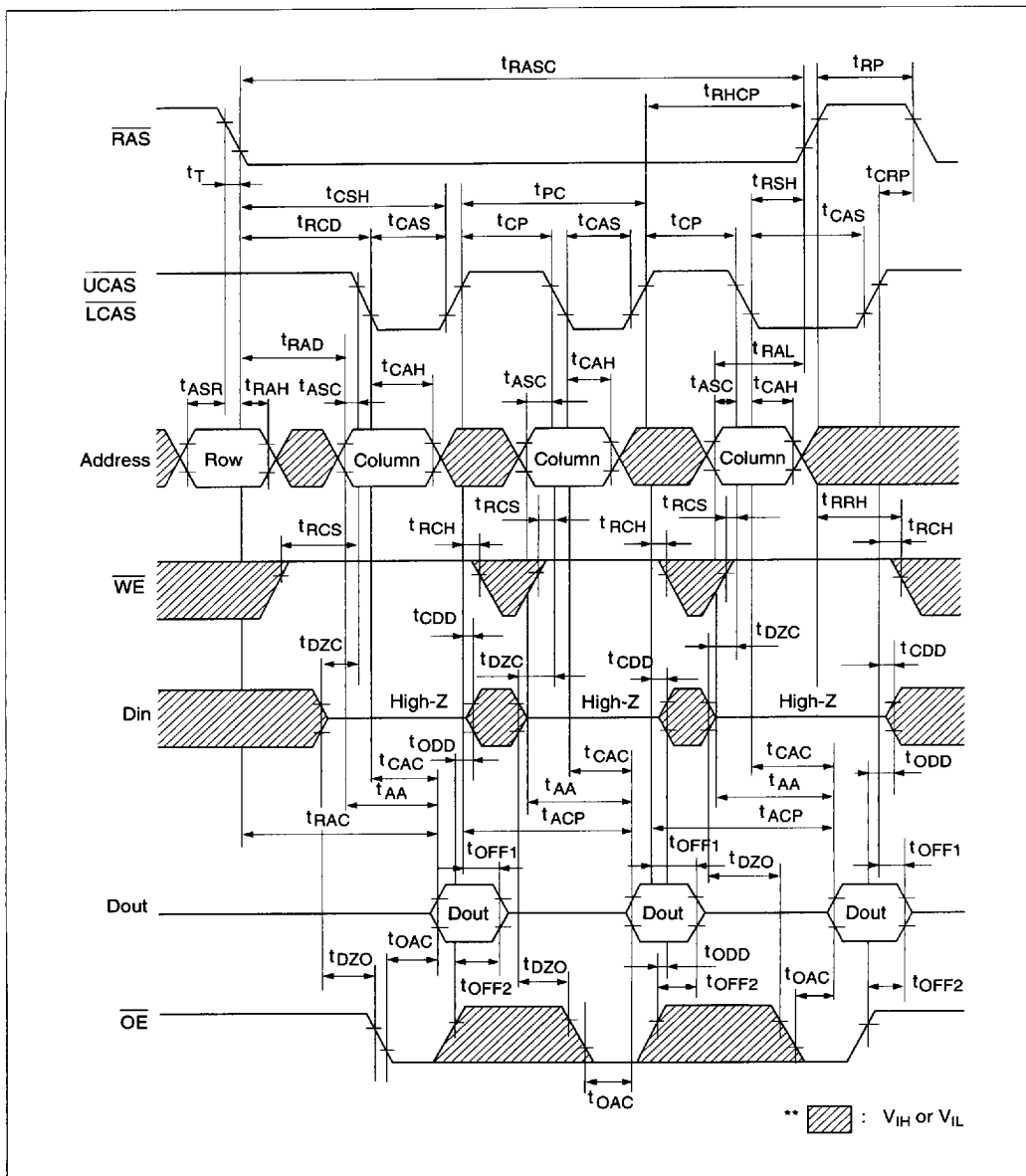
CAS-Before-RAS Refresh Cycle



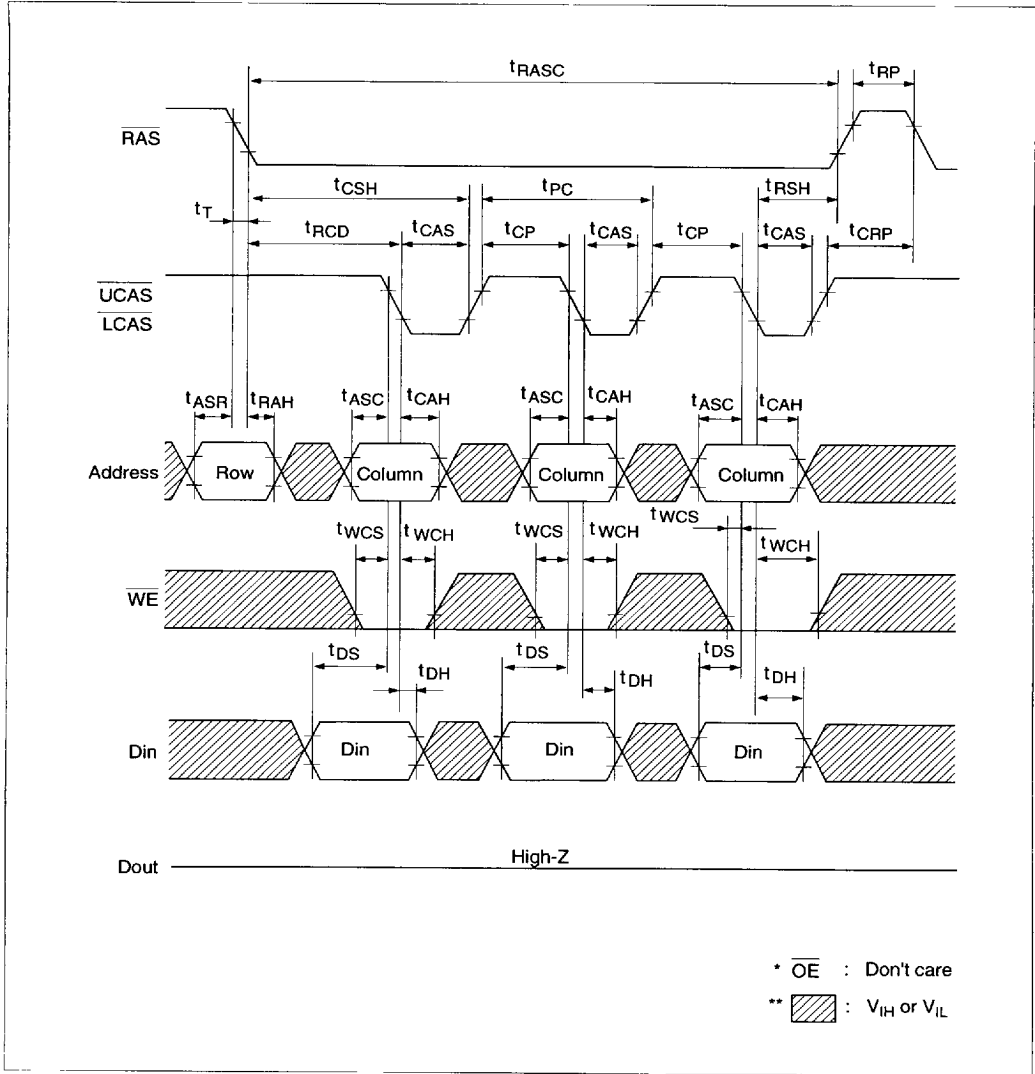
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HM51W4260A/AL Series

Fast Page Mode Read Cycle



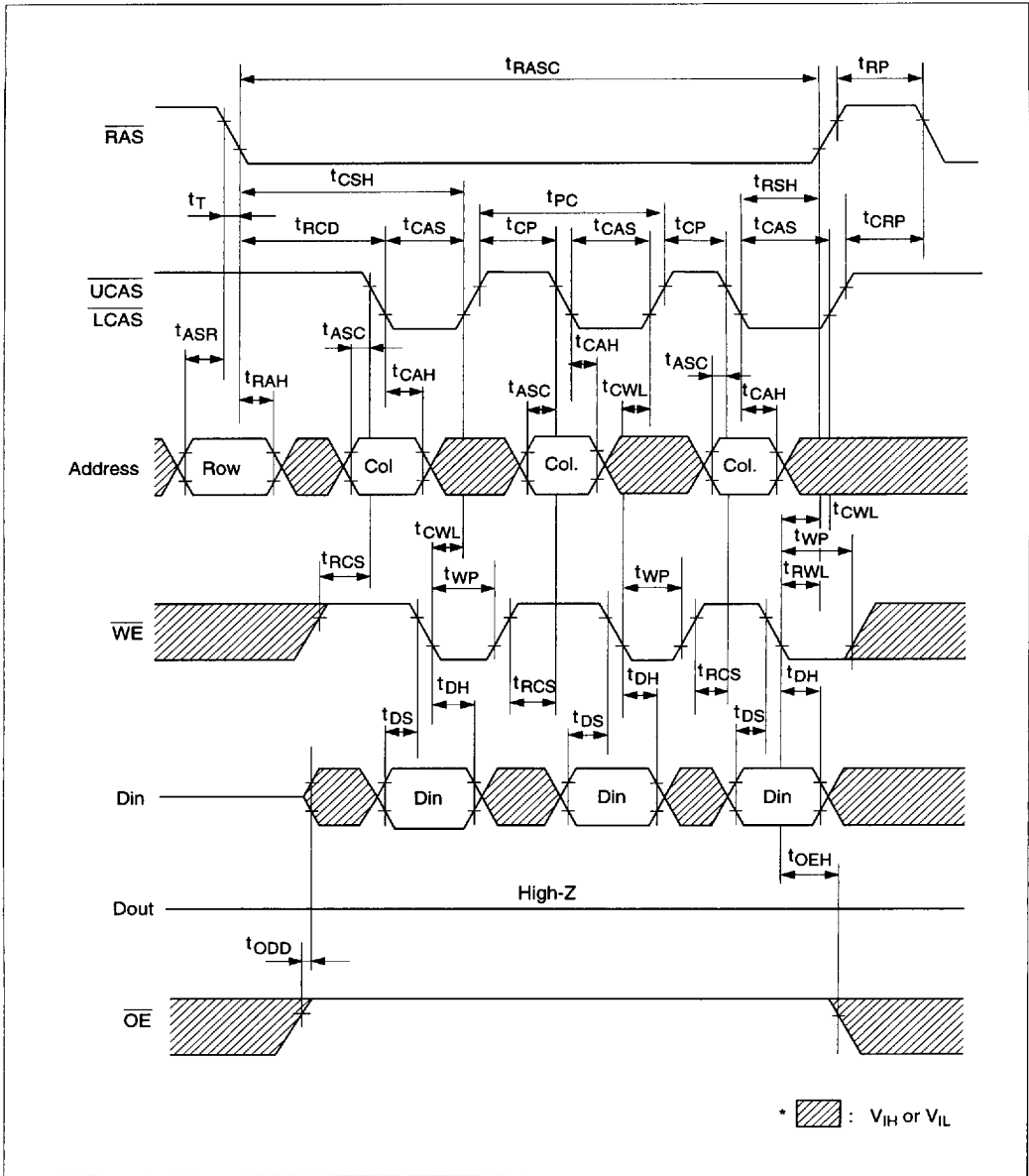
Fast Page Mode Early Write Cycle



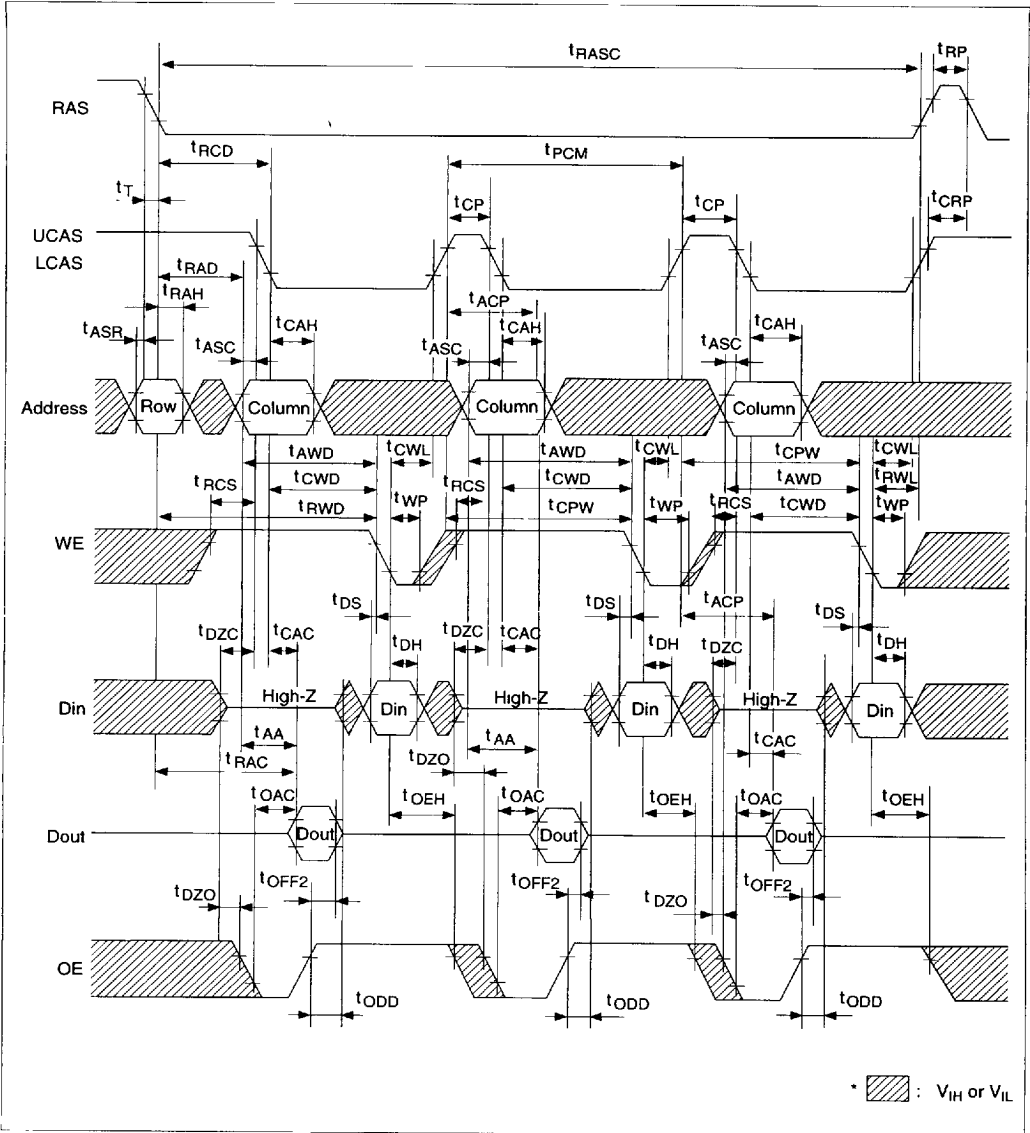
4496203 0026690 439

HM51W4260A/AL Series

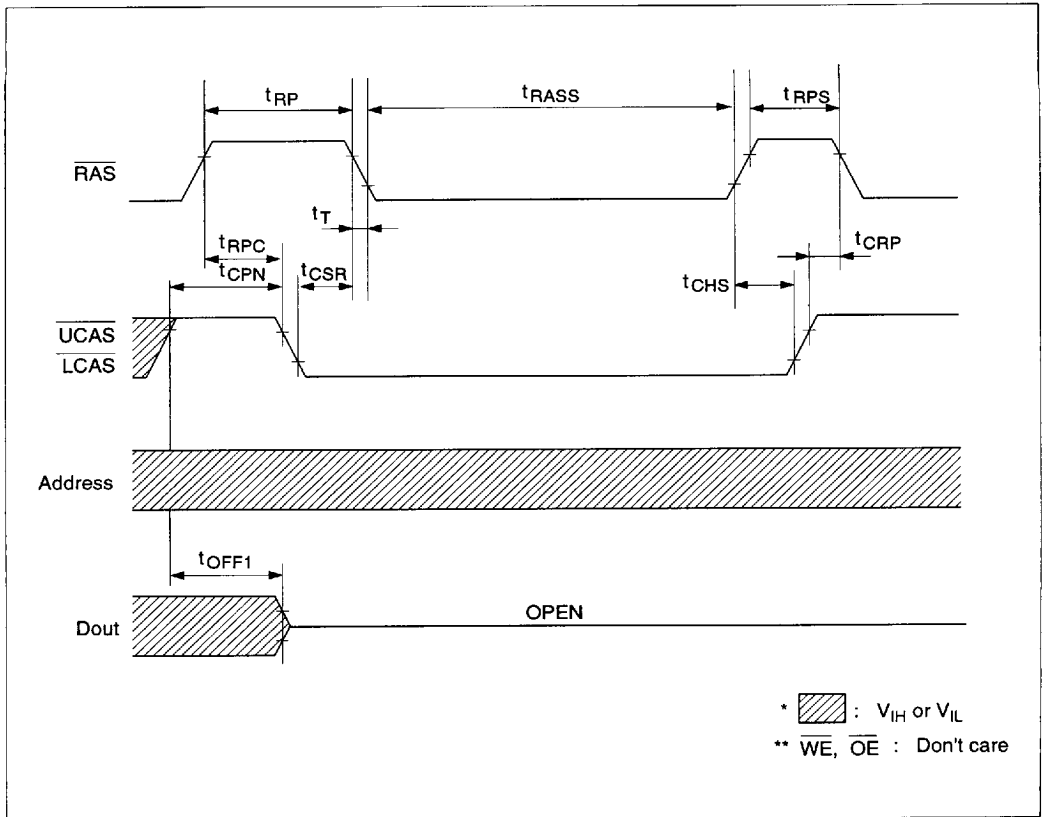
Fast Page Mode Delayed Write Cycle



Fast Page Mode Read-Modify-Write Cycle



Self Refresh Cycle



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then \overline{RAS} precharge time should use t_{RPS} instead of t_{RP} .
2. If you use \overline{RAS} only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with $15.6 \mu s$ interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with $15.6 \mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6 \mu s$ immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.